Listing of Claims:

1. (original) An integrated circuit including a metal fill pattern comprising:

a first plurality of metal traces electrically connected to a power supply pad; and

a second plurality of metal traces electrically connected to a ground pad;

wherein said second plurality of metal traces are interdigitated between said first plurality of metal traces to form a purposeful inter-metal capacitance therebetween.

2. (original) The integrated circuit including a metal fill pattern according to claim 1, wherein:

said first plurality of metal traces and said second plurality of metal traces further function as a purposeful shield to minimize electromagnetic radiation from affecting circuitry therebelow.

3. (original) The integrated circuit including a metal fill pattern according to claim 2, wherein:

said circuitry therebelow includes an analog circuit.

4. (original) The integrated circuit including a metal fill pattern according to claim 1, further comprising:

a first plurality of traces crossing each of said first plurality of metal traces; and

a second plurality of traces crossing each of said second plurality of metal traces.

5. (original) The integrated circuit including a metal fill pattern according to claim 4, wherein:

said first plurality of traces each form a perpendicular angle with respect to an electrically connected one of said first plurality of metal traces.

6. (original) The integrated circuit including a metal fill pattern according to claim 5, wherein:

said second plurality of traces each form a perpendicular angle with respect to an electrically connected one of said second plurality of metal traces.

7. (original) The integrated circuit including a metal fill pattern according to claim 5, wherein:

a portion of said first plurality of metal traces connected to a number of said first plurality of traces forms a straight line.

8. (original) The integrated circuit including a metal fill pattern according to claim 5, wherein:

a portion of said first plurality of metal traces connected to a number of said first plurality of traces forms a curving line.

9. (original) The integrated circuit including a metal fill pattern according to claim 7, wherein:

another portion of said first plurality of metal traces connected to others of said first plurality of traces forms a curving line.

10. (original) The integrated circuit including a metal fill pattern according to claim 1, wherein:

said metal fill pattern forms a coverage density of at least 50%.

11. (original) The integrated circuit including a metal fill pattern according to claim 1, wherein:

said first plurality of metal traces and said second plurality of metal traces are linear.

12. (original) The integrated circuit including a metal fill pattern according to claim 11, wherein:

said first plurality of metal traces and said second plurality of linear metal traces run along a generally straight line.

13. (original) A method of forming a cross-fill metal fill pattern in an integrated circuit that provides a plurality of purposeful functions, comprising:

forming a first plurality of parallel traces electrically connected;

forming a second plurality of parallel traces electrically connected;

electrically routing said first plurality of parallel traces to a common power rail in said integrated circuit; and

electrically routing said second plurality of parallel traces to a common ground rail in said integrated circuit;

wherein said cross-fill metal pattern provides metal fill as a first purposeful function, and as a second purposeful function provides at least one of capacitance across a power supply, and electro-magnetic shielding to protect an analog circuit therebelow.

14. (original) The method of forming a metal fill pattern in an integrated circuit that provides a plurality of purposeful functions according to claim 13, further comprising:

forming interdigitated fingers physically connected to at least one of said first plurality of parallel traces; and

forming interdigitated fingers physically connected to at least one of said second plurality of parallel traces.

15. (original) The method of forming a metal fill pattern in an integrated circuit that provides a plurality of purposeful functions according to claim 13, wherein:

said cross-fill metal pattern achieves three purposeful functions of (1) providing metal fill, (2) provides decoupling capacitance across a power supply when powering said integrated circuit, and (3) provides an electro-magnetic shield to protect an analog circuit therebelow.

16. (original) Apparatus for forming a cross-fill metal fill pattern in an integrated circuit that provides a plurality of purposeful functions, comprising:

means for forming a first plurality of parallel traces electrically connected;

means for forming a second plurality of parallel traces electrically connected;

means for electrically routing said first plurality of parallel traces to a common power rail in said integrated circuit; and

means for electrically routing said second plurality of parallel traces to a common ground rail in said integrated circuit;

wherein said cross-fill metal pattern provides metal fill as a first purposeful function, and as a second purposeful function provides at least one of capacitance across a power supply, and electro-magnetic shielding to protect an analog circuit therebelow.

17. (original) The apparatus for forming a metal fill pattern in an integrated circuit that provides a plurality of purposeful functions according to claim 16, further comprising:

means for forming interdigitated fingers physically connected to at least one of said first plurality of parallel traces; and

means for forming interdigitated fingers physically connected to at least one of said second plurality of parallel traces.

18. (original) The method of forming a metal fill pattern in an integrated circuit that provides a plurality of purposeful functions according to claim 16, wherein:

said cross-fill metal pattern achieves three purposeful functions of (1) providing metal fill, (2) provides decoupling capacitance across a power supply when powering said integrated circuit, and (3) provides an electro-magnetic shield to protect an analog circuit therebelow.